Amendments to the Drawings:

The attached drawing sheets include changes to Figures 1 and 3. In Figure 1, reference tag 104 is added to identify the storage circuit 104. The omission of reference tag 104 was a typographical error, which is corrected by this amendment.

In Figure 3, reference tag 325 is added to identify the OR gate 325. Additionally, reference tags 326 and 391 replace incorrect reference tags in the original drawings. These changes correct typographical errors in the original drawings.

REMARKS/ARGUMENTS

In the Office Action mailed February 12, 2008, claims 1-35 were rejected. Additionally, the specification was objected to. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are amended, added, or canceled.

For reference, Figures 1 and 3 are amended to correct typographical errors.

Objections to the Specification

The Office Action suggests that section headings be added to the specification according to the guidelines set forth in the MPEP. Applicants note that the suggested section headings are not required and, hence, Applicants respectfully decline to amend the specification to include the indicated section headings.

Additionally, the Office Action objects to the specification as failing to provide proper antecedent basis for the "frequency compensation code," "skip code," and "comma code" recited in claims 1, 4, and 26 and "data symbols" in claim 26. The rule, 37 C.F.R. 1.75(d)(1), requires that terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable. In other words, support is required, and antecedent basis is simply one way of providing support, but antecedent basis is not the only way to provide support for the limitations of the claim. Further, MPEP 608.01(o) recognizes that an applicant is not limited to the nomenclature used in the application as filed. Hence, the MPEP also recognizes that the language of the claims does not have to be explicitly, or literally, supported by the description of the specification.

In the present application, the originally filed claims 1, 4, 24, and 26 include the indicated language related to the frequency compensation code, skip code, comma code, and data symbols. Moreover, the claims are part of the specification. Although the detailed description section of the specification may use language other than the exact terminology recited in the claims, Applicants submit that the specification otherwise supports the indicated language, at least because the originally filed claims include the indicated language and are part of the originally filed specification.

Additionally, Applicants submit that the specification otherwise supports the indicated language. Specifically, one use of the term "frequency compensation code" is clearly understood in the specification as a code "used for frequency compensation." Page 6, lines 3-5. One use of the term "skip code" refers to a specific sequence of data symbols that may be used in a frequency compensation code. Page 6, lines 4-6. One use of the term "comma code" refers to another specific sequence of data symbols that may be used in a frequency compensation code. Page 10, lines 20-23. Comma codes and skip codes are also described in Gregg et al. (U.S. Pat. No. 5,598,442, hereinafter Gregg). Gregg, column 2, lines 42-50. "Data symbols" may be interpreted using the common meaning of the individual words, as used within the context of the present application. Specifically, a data symbol may be a symbol used to communicate data. Accordingly, Applicants respectfully requests that the objections to the specification be withdrawn.

If the Examiner persists in this line of reasoning, Applicants would consider amending the specification to include at least some of the language from one or more of claims 1, 4, 23, and 26. While such an amendment to the specification would be supported by the language of the originally filed claims, it would seem to be an unnecessary exercise in light of the language of the originally filed claims. Nevertheless, Applicants are amenable to resolving this issue raised by the Examiner.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1-4, 22-25, 26, 27, 29, and 30 were rejected under 35 U.S.C. 102(b) as being anticipated by Gregg. Additionally, claims 5-11, 28, and 31-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg in view of Imanishi (U.S. Pat. No. 5,974,055, hereinafter Imanishi). Additionally, claims 12-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg in view of Wakeman et al. (U.S. Pat. No. 5,790,786, hereinafter Wakeman). However, Applicants respectfully submit that these claims are patentable over Gregg, Imanishi, and Wakeman for the reasons provided below. For convenience, the claims are discussed in substantially the order presented by the Examiner in the Office Action.

Independent Claim 1

Claim 1 recites "a receive module . . . adapted to detect therein a frequency compensation code and, in response thereto, align the data carried from the transmit module" (emphasis added).

In contrast, Gregg does not disclose aligning data in response to a frequency compensation code. Gregg merely discloses "examin[ing] the characters to determine if all of the conductors have achieved character synchronism." Gregg, column 4, lines 16-17, emphasis added. Gregg further describes "tak[ing] the link out of the sync acquired state" (column 4, lines 23-24) in response to detecting an "error" (column 4, lines 21-22) and discarding bits from the bit streams (column 4, lines 30-32) until determining if a "sync acquired" state is entered (column 4, lines 32-41). In other words, Gregg discloses detecting and discarding out of sync data. Nevertheless, Gregg does not describe aligning out of sync data in response to a frequency compensation code as recited in claim 1.

The Office Action cites Figure 2, Element 54, as purportedly disclosing aligning the data carried from the transmit module. Figure 2, Element 54 is labeled "DESER/ALIGN/CHAR SYNC" and described as "a logic array 54 that deserializes each input, and aligns and synchronizes the characters among the four inputs, as explained in greater detail in connection with FIG. 4." Gregg, column 3, lines 30-33. The description of FIG. 4 discloses detecting and discarding out of sync data, as described above. However, the description of FIG. 4 does not disclose aligning out of sync data in response to a frequency compensation code as recited in claim 1.

Gregg further discloses that "data streams are aligned by searching for the idle pattern." Gregg, column 3, line 34. In other words, Gregg discloses attempting to align data streams by searching for corresponding portions of each data stream where no data is being transmitted. Gregg does not disclose aligning data in response to an explicit frequency compensation code and, therefore, would not be able to align data without the presence of portions of the data stream where no data is being transmitted. Furthermore, data streams having a high frequency of portions of the data stream where no data is being transmitted may result in a misalignment using the invention in Gregg, as it provides no method of distinguishing between "idle patterns."

Gregg at no point discloses the use of a frequency compensation code to align the data. Gregg limits the use of skip codes to the activation of a "SKIP" function "that can discard a bit from the data stream." Gregg, column 3, lines 51-52. Gregg does not disclose using a code, such as a skip code, to align the data streams. Therefore, Gregg does not disclose the use of a frequency compensation code to align data, as recited in claim 1, because Gregg merely teaches discarding out of sync data and aligning data by searching for idle patterns.

For the reasons presented above, Gregg does not disclose all of the limitations of the claim because Gregg does not disclose aligning data in response to a frequency compensation code, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over Gregg because Gregg does not disclose all of the limitations of the claim.

Independent Claim 22

Applicants respectfully assert independent claim 22 is patentable over Gregg at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 22 recites "means for converting serial data streams from a plurality of byte lanes into parallel data, wherein the parallel data is aligned using the frequency compensation code" (emphasis added).

Here, although the language of claim 22 differs from the language of claim 1 and the scope of claim 22 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 22. Accordingly, Applicants respectfully assert claim 22 is patentable over Gregg because Gregg does not disclose aligning data using a frequency compensation code.

Independent Claim 26

Applicants respectfully assert independent claim 26 is patentable over Gregg at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 26 recites "an alignment circuit adapted to respond to the codes by aligning the data symbols and by removing the codes" (emphasis added).

Here, although the language of claim 26 differs from the language of claim 1 and the scope of claim 26 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 26. Accordingly, Applicants respectfully assert claim 26 is patentable over Gregg because Gregg does not disclose aligning data symbols in response to codes.

Independent Claim 8

Claim 8 recites "an alignment storage circuit . . . adapted to provide an alignment detection signal to a data shift circuit in response to detection of the frequency compensation code for each portion of data received, and adaptively shift the parallel data output from the portions of data in response to the alignment detection signal" (emphasis added).

In contrast, Gregg does not teach adaptively shifting parallel data output in response to a frequency compensation code. It should be noted that even though the claim is rejected based on the combination of Gregg and Imanishi, the Office Action merely relies on the purported teachings of Gregg. Since the Office Action does not assert any teachings by Imanishi related to the indicated limitation of the alignment storage circuit, Applicants' response is presented as fully responsive by showing that Gregg does not teach the indicated limitation.

The Office Action cites Figure 3, signal 69, as purportedly teaching adaptively shifting parallel output in response to the alignment detection signal. Reference character 69 is described in Gregg as a "bit position" (column 3, lines 61-62) that indicates the boundary of a K28.5 character (column 4, lines 1-2). The K28.5 character is described as an idle sequence. Gregg, column 2, lines 43-44.

As described above in relation to claim 1, Gregg teaches attempting to align data streams by searching for corresponding portions of each data stream where no data is being transmitted. Gregg does not teach aligning data in response to an explicit frequency compensation code. Consequently, Gregg does not teach adaptively shifting parallel data output in response to a frequency compensation code as recited in claim 8, because Gregg merely teaches attempting to align data by searching for idle patterns.

For the reasons presented above, Gregg does not teach all of the limitations of the claim because Gregg does not teach adaptively shifting parallel data output in response to a frequency compensation code, as recited in the claim. Accordingly, Applicants respectfully assert claim 8 is patentable over Gregg, whether considered alone or in combination with Imanishi, because Gregg does not teach all of the limitations of the claim.

Independent Claim 12

Claim 12 recites "the alignment storage circuit adapted to provide an alignment detection signal to a data shift circuit in response to detection of a frequency compensation code for each serial bit-stream" (emphasis added). As stated by the Examiner, Gregg does not disclose this limitation. The Office Action states, however, that "Wakeman discloses . . . the alignment storage circuit adapted to provide an alignment detection signal to a data shift circuit (Column 3, Lines 19-25) in response to detection of a frequency compensation code for each serial bit-stream." Office Action, page 13.

Wakeman, however, does not teach the use of a frequency compensation code. Wakeman merely states that "each receive data path circuit starts latching data signals from a network bus into a shift register independent of the availability of the received data path controller . . . each receive data path circuit includes a shift register having a length of 2n, wherein n is the number of bus cycles that occur on a receive input terminal during a cycle period." Wakeman, column 3, lines 19-29. In other words, the "latching" described in Wakeman is controlled by a number of bus cycles. Since the latching is controlled by a number of bus cycles, the latching is not in response to detection of a frequency compensation code as recited in claim.

For the reasons presented above, neither Gregg nor Wakeman teaches all of the limitations of the claim because neither Gregg nor Wakeman teaches providing an alignment detection signal to a data shift circuit in response to detection of a frequency compensation code, as recited in the claim. Accordingly, Applicants respectfully assert claim 12 is patentable over Gregg and Wakeman.

Independent Claim 19

Applicants respectfully assert independent claim 19 is patentable over Gregg and Wakeman at least for similar reasons to those stated above in regard to the rejection of independent claim 12. In particular, claim 19 recites "converting serial data streams from the plurality of byte lanes into parallel data, wherein the parallel data is aligned using the frequency compensation codes" (emphasis added).

Here, although the language of claim 19 differs from the language of claim 12 and the scope of claim 19 should be interpreted independently of claim 12, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of claim 19. Accordingly, Applicants respectfully assert claim 19 is patentable over Gregg and Wakeman because neither Gregg nor Wakeman teaches aligning data using frequency compensation codes.

Independent Claim 32

Claim 32 recites "receiving the plurality of serial bit-streams[, and] performing a one-bit shift of the least one of the bit-streams" (emphasis added). As stated by the Examiner, Gregg does not disclose this limitation. The Office Action states, however, that "Imanishi discloses the method of performing a one-bit shift of the at least one of the bit-streams (Figure 12, Shift Reg. 47)." Office Action, page 10.

Imanishi, however, does not teach shifting a serial bit-stream by one bit as recited in claim 1. Imanishi teaches multiplexing/demultiplexing for the transmission of several signals over a single transmission path. Imanishi, Abstract. In other words, Imanishi involves transmitting several independent data signals over a single transmission path for later separation, and the data operated on by the shift registers 47 is not a serial bit stream, but a parallel stream including a plurality of signals. Imanishi, FIG. 6. Therefore, Imanishi also fails to teach performing a one-bit shift on a serial bit-stream.

The Office Action also states that the "suggestion/motivation for [modifying Gregg to include Imanishi] what had been to improve design flexibility." Office Action, page 11. Such a bare, conclusory statement does not present a sufficient motivation to combine two references. "[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some

rational underpinning to support the legal conclusion of obviousness." MPEP 2143.01 IV. It is not clear that the modification does, in fact, "improve design flexibility," or indeed, what "design flexibility" means.

Since neither Gregg nor Imanishi teach performing a one-bit shift on a serial bit-stream, Applicants submit that claim 32 is not obvious under Gregg in view of Imanishi. Furthermore, as a separate basis for patentability, Applicants submit that the Office Action does not describe a sufficient teaching, suggestion, or motivation for combining Gregg and Imanishi. Consequently, Applicants respectfully assert claim 32 is patentable over Gregg and Imanishi.

Dependent Claims

Claims 2-7, 9-11, 13-18, 20, 21, 23-25, 27-31, and 33-35 depend from and incorporate all of the limitations of the corresponding independent claims 1, 8, 12, 19, 22, 26, and 32. Applicants respectfully assert claims 2-7, 9-11, 13-18, 20, 21, 23-25, 27-31, and 33-35 are allowable based on allowable base claims. Additionally, each of claims 2-7, 9-11, 13-18, 20, 21, 23-25, 27-31, and 33-35 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/Jeffrey T. Holman/

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Jeffrey T. Holman
Reg. No. 51,812

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111